

AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of the claims:

1. (Previously Presented) A memory cell of a semiconductor device, comprising:
 - a substrate having active regions and field regions;
 - a gate layer formed over the substrate, the gate layer including a plurality of access gates formed over the active regions of the substrate and a plurality of pass gates formed over the field regions of the substrate;
 - first self-aligned contact regions (**BC SAC region**) formed between adjacent pass gates and access gates; and
 - second self-aligned contact regions (**DC SAC region**) formed between adjacent access gates,
 - wherein a width of each of the first self-aligned contact regions is larger than a width of each of the second self-aligned contact regions, and
 - wherein the width of each of the first self-aligned contact regions is made larger than the width of each of the second self-aligned contact regions by each one of the plurality of access gates having a width smaller than a width of an adjacent pass gate.
2. (Canceled).
3. (Previously Presented) The memory cell of a semiconductor device as claimed in claim 1, wherein a ratio of the width of the first self-aligned contact region to the width of the second self-aligned contact region is in a range from greater than 1.0 up to 1.2.

4. (Previously Presented) The memory cell of a semiconductor device as claimed in claim 3, wherein the ratio of the width of the first self-aligned contact region to the width of the second self-aligned contact region is approximately 1.1.

5. (Original) The memory cell of a semiconductor device as claimed in claim 1, further comprising:
sidewall spacers formed on sidewalls of each of the plurality of access gates and each of the plurality of pass gates.

6. (Original) The memory cell of a semiconductor device as claimed in claim 5, further comprising:
a recess hole having an opening and a bottom for receiving one of the plurality of access gates, wherein a width of the opening of the recess hole is larger than a width of the bottom of the recess hole.

7. (Original) The memory cell of a semiconductor device as claimed in claim 6, wherein the sidewall spacers formed on sidewalls of the plurality of access gates extend below an upper surface of the substrate.

8. (Currently Amended) The memory cell of a semiconductor device as claimed in claim 5, further comprising:
an interlayer dielectric layer formed over a pass gate ~~[[the]]~~ sidewall spacer ~~formed on the sidewall of one of the plurality of pass gates~~ and the field region of the substrate.

9. (Original) The memory cell of a semiconductor device as claimed in claim 2, wherein the width of each of the plurality of access gates is decreased by a notch formed on at least one side of each of the plurality of access gates.

10. (Original) The memory cell of a semiconductor device as claimed in claim 9, wherein the notch has a depth of between about 10 - 20 nm.

11. (Original) The memory cell of a semiconductor device as claimed in claim 9, wherein the notch formed on at least one side of each of the plurality of access gates is formed adjacent to the first self-aligned contact region so as to face one of the plurality of pass gates.

12. (Original) The memory cell of a semiconductor device as claimed in claim 9, wherein the notch formed on at least one side of each of the plurality of access gates is formed adjacent to the second self-aligned contact region so as to face one of the plurality of access gates.

13. (Original) The memory cell of a semiconductor device as claimed in claim 9, wherein each of the plurality of access gates has a pair of notches, each notch formed on opposing sides of each of the plurality of access gates.

14-21. (Canceled).

AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings include proposed changes to FIGS. 2, 7 and 12. The attached drawing sheets of FIGS. 2, 7 and 12 replace the original drawing sheets of FIGS. 2, 7 and 12. In FIG. 2, reference numeral 130a now indicates the intersection and --100b-- has been added to indicate the field region. In FIG. 7, reference numeral 230a now indicates the intersection and --200b-- has been added to indicate the field region. In FIG. 12, reference numeral 330a now indicates the intersection and --300b-- has been added to indicate the field region.

Applicants respectfully request favorable review and approval of the proposed amendments to the drawings.

Attachment: Replacement Drawing Sheets of FIGS. 2, 7 and 12

Annotated Drawing Sheet Showing Proposed Changes